REMARKS

Applicants have carefully reviewed this application in light of the Final Office Action mailed September 12, 2005. Applicants appreciate the Examiner's consideration of the Application and respectfully request favorable action in this case.

Interview Summary

Applicants' attorney Jeff Baxter and Examiner Ricardo Pizarro had a telephone interview on November 11, 2005. Mr. Baxter pointed out that the Examiner had not responded to Applicants' argument for allowance and, in particular, to Applicants' argument that U.S. Patent No. 6,463,414 ("*Su*") is not prior art under § 102(a). The Examiner agreed that *Su* is not prior art under § 102(a). The Examiner further agreed that *Su* is prior art under § 102(e) only to the extent its disclosure is supported by Provision Application No. 09/547,832. The Examiner stated that he had not reviewed the provisional application, which Applicants submitted in conjunction with a prior response. The Examiner requested that Applicants file a response to the Final Office Action including a summary of the interview, and in response, the Examiner would consider the provisional application.

Applicants' attorney also pointed out that the Examiner's claims rejections based on *Su* were inconsistent with the Examiner's reading of *Su* as not disclosing separate processors. Applicants' attorney also pointed out the passages from *Su* quoted in Applicants' prior responses that demonstrate that *Su* describes functional blocks as opposed to separate processors.

Claim Rejections -- 35 U.S.C. § 102

The Examiner rejected Claims 38, 2–4, 7 39, 9–11, 14, 40, 32–34, and 37 under 35 U.S.C. §102(a) as being anticipated by U.S. Patent No. 6,463,414 ("*Su*").

Su issued after Applicants' filing date and thus is not prior art under 35 U.S.C. § 102(a).

Furthermore, *Su* is not prior art under § 102(e) because it was filed on April 12, 2000, which is almost four months after Applicants' filing date of December 15, 1999. While *Su* claims priority to a provisional application filed on April 12, 1999, that provisional application does not support the entire disclosure of *Su*. *Su* may qualify as prior art only to the extent the disclosure is supported by Provision Application No. 09/547,832 ("*Su*

Provisional Application"), which Applicants previously submitted for the Examiner's consideration.

Independent Claim 38 and Dependent Claims 2-7

Independent Claim 38, as amended, recites:

> An apparatus for using a plurality of processors to support a media conference, comprising:
>
> a mixing processor operable to mix input media information associated with two or more first participants to generate output media information for communication to a second participant; and
>
> a first media transformation processor coupled to the mixing processor, the first media transformation processor operable to receive the output media information from the mixing processor, to encode the output media information to generate an output data stream, and to communicate the output data stream to the second participant's end-user device,
>
> wherein the mixing processor and the first media transformation processor are separate hardware components.

The Examiner's rejections are based on Figures 2 and 5 of *Su*, and these figures are not prior art because they are not included in the *Su Provisional Application*. Figure 2 of the *Su Provisional Application* (which may or may not be prior art) clearly portrays the decoding, mixing, and re-encoding as functional blocks as opposed to separate hardware components.

Moreover, *Su* does not disclose, teach, or suggest Applicants' claimed invention because, as the Examiner has acknowledged, *Su* does not disclose separate processors as recited in Claim 38. Independent Claims 38 requires a "mixing processor" and a "first media transformation processor" and, as stated in the claim, "the mixing processor and the first media transformation processor are separate hardware components."

The Examiner has several times acknowledged that *Su* does not disclose separate processors. In the Office Action mailed March 1, 2005 and the Final Office Action mailed September 12, 2005, the Examiner stated:

> Su did not specifically disclose said processors being separate as in claims 5, 12, and 35, being DSP as in claim 6, 13 and 36.

(p. 6) (emphasis added). While the Examiner later states in the Final Office that this statement is referring only to the DSP processors, that is plainly not true. The Examiner has

stated that, in addition to not disclosing DSP as in Claims 6, 13, and 36, *Su* also does not disclose the "processors being separate as in claims 5, 12, and 35."

Furthermore, the written description of *Su* confirms that *Su* does not disclose the "processors being separate as in claims 5, 12, and 35" as stated by the Examiner. *Su* expressly states that the invention is described in terms of "functional block components" which may be implemented using "any number of hardware components or software elements":

> The present invention may be described herein in terms of functional block components and various processing steps. It should be appreciated that such functional blocks may be realized by any number of hardware components or software elements configured to perform the specified functions. For example, the present invention may employ various integrated circuit components, e.g., memory elements, digital signal processing elements, logic elements, look-up tables, and the like, which may carry out a variety of functions under the control of one or more microprocessors or other control devices.

(Col. 2, ll. 49-59) (emphasis added). *Su* does not specify that the functions of decoders 230 and 234, mixer 238 and 240, and encoder 232 and 236 are assigned to separate processors. Indeed, *Su* provides that the functional blocks may be implemented in software.

Another passage in *Su* further indicates that Figure 2, on which the Examiner relies to support the rejections, is a "simplified schematic" of functional blocks as opposed to hardware components.

> FIG. 2 is a simplified schematic: there might also be certain additional components advantageously coupled between the packet network and the decoders (and encoders). Specifically, with respect to the decoders, there. will likely be a functional block (not shown) that receives the packets from packet network 201 and removes all unnecessary routing, encryption, and protection information (a "decapsulator"). Conversely, with respect to the encoders, there will likely be a functional block (an "encapsulator") for each encoder that receives speech samples from the mixer and adds certain information regarding routing, encryption, and the like prior to sending the packets out over packet network 201.

(Col. 5, ll. 19-31) (emphasis added).

For at least these reasons, *Su* does not disclose, teach, or suggest the "mixing processor" and "first media transformation processor," "wherein the mixing processor and the first media transformation processor are separate hardware components," as recited in Claim

38. Accordingly, Applicants respectfully request reconsideration and allowance of independent Claims 38, as well as Claims 2-7 which depend from Claim 38.

Independent Claim 39 and Dependent Claims 9-14

Independent Claim 39, as amended, recites:

> A method for using a plurality of processors to support a media conference, comprising:
>
> mixing input media information associated with two or more first participants to generate output media information for communication to a second participant using a mixing processor;
>
> communicating the output media information from the mixing processor to a first media transformation processor, wherein the mixing processor and the first media transformation processor are separate hardware components;
>
> encoding the output media information to generate an output data stream using the first media transformation processor; and
>
> communicating the output data stream from the first media transformation processor to the second participant's end-user device.

The Examiner's rejections are based on Figures 2 and 5 of *Su*, and these figures are not prior art because they are not included in the *Su Provisional Application*. Figure 2 of the *Su Provisional Application* (which may or may not be prior art) clearly portrays the decoding, mixing and re-encoding as functional blocks as opposed to separate hardware components.

Su does not disclose, teach, or suggest Applicants' claimed invention because, as the Examiner acknowledged in the Office Action, *Su* does not disclose separate processors as recited in Claim 39. Like Claims 38, independent Claim 39 requires multiple processors. Claim 39 recites the steps "mixing input media information associated with two or more first participants to generate output media information for communication to a second participant using a mixing processor," "communicating the output media information from the mixing processor to a first media transformation processor, wherein the mixing processor and first media transformation processor are separate hardware components," and "encoding the output media information to generate an output data stream using the first media transformation processor." Because *Su* and the *Su Provisional Application* disclose

functional blocks as opposed to separate processors, *Su* does not disclose, teach, or suggest the "mixing processor" and "first media transformation processor," "wherein the mixing processor and the first media transformation processor are separate hardware components," as recited in Claim 39. Accordingly, Applicants respectfully request reconsideration and allowance of independent Claims 39, as well as Claims 9-14 which depend from Claim 39.

Independent Claim 40 and Dependent Claims 32-34 and 37

Independent Claim 40, as amended, recites:

> A system for using a plurality of processors to support a media conference, comprising:
>
> a plurality of end-user devices coupled to a data network and operable to generate input media information, to encode the input media information to generate input data streams, and to communicate the input data streams using the data network; and
>
> a conferencing device coupled to the data network, the conferencing device comprising two or more processors operable to decode the input data streams to generate the input media information, to mix the input media information to generate output media information, and to encode the output media information to generate output data streams, wherein the processors are separate hardware components;
>
> wherein the end-user devices are further operable to receive the output data streams and to decode the output data streams to generate output media information

The Examiner's rejections are based on Figures 2 and 5 of *Su*, and these figures are not prior art because they are not included in the *Su Provisional Application*. Figure 2 of the *Su Provisional Application* (which may or may not be prior art) clearly portrays the decoding, mixing and re-encoding as functional blocks as opposed to separate hardware components.

Su does not disclose, teach, or suggest Applicants' claimed invention because, as the Examiner acknowledged in the Office Action, *Su* does not disclose separate processors as recited in the claims. Like Claims 38 and 39, independent Claim 40 requires multiple processors. Claim 40 recites, "the conferencing device comprising two or more processors operable to decode the input data streams to generate the input media information, to mix the input media information to generate output media information, and to encode the output media information to generate output data streams, wherein the processors are separate hardware components." Because *Su* and the *Su Provisional Application* disclose functional

blocks as opposed to separate processors, *Su* does not specify that the functions of decoders 230 and 234, mixer 238 and 240, and encoder 232 and 236 are assigned to separate processors. For at least this reason, *Su* does not disclose, teach, or suggest "the conferencing device comprising two or more processors operable to decode the input data streams to generate the input media information, to mix the input media information to generate output media information, and to encode the output media information to generate output data streams, wherein the processors are separate hardware components," as recited in Claim 40. Accordingly, Applicants respectfully request reconsideration and allowance of independent Claims 40, as well as Claims 32-34 and 37 which depend from Claim 40.

Claim Rejections -- 35 U.S.C. § 103

The Examiner rejected Claims 5, 6, 12, 13, 35, and 36 under 35 U.S.C. § 103 as being unpatentable over *Su* in view of U.S. Patent 5,841,763 ("*Leondires*").

According to the Examiner, *Leondires* "discloses a conferencing device with separate processors." (p. 6). *Leondires*, however, does not disclose, teach, or suggest using separate processors for mixing and encoding. The portion of the specification cited by the Examiner describes audio decoding digital signal processors (ADPs) and audio encoding digital signal processors (AEPs). The ADPs decode audio information. (Col. 14, ll. 33-43). The AEPs mix and encode audio information: "The AEPs read the decoded audio signals from DSs time slots, mix the decoded audio signals from each of the conferees and encode the results of the mixing according to the particular G-series standard." (Col. 14, ll. 51-54). Thus, *Leondires* expressly teaches away from Applicants' claimed invention.

In contrast to the AEPs of *Leondires*, Claims 38 and 39 require two separate processors for mixing and encoding. Claim 39 requires: (1) "a mixing processor operable to mix input media information" and (2) "first media transformation processor operable to receive the output media information from the mixing processor, to encode the output media information to generate an output data stream, and to communicate the output data stream to the second participant's end-user device." Similarly, Claim 39 distinguishes between a mixing processor for mixing and a media transformation processor for encoding. Claim 39 requires the following steps: "mixing input media information associated with two or more first participants to generate output media information for communication to a second participant," "communicating the output media information from a mixing processor to a first

media transformation processor," and "encoding the output media information to generate an output data stream."

For the reasons discussed above with respect to independent Claims 38, 39, and 40, as well as these additional reasons, *Su* and *Leondires* do not disclose Applicants' claimed invention recited in dependent Claims 5, 6, 12, 13, 35, and 36. Accordingly, Applicants respectfully request reconsideration and allowance of dependent Claims 5, 6, 12, 13, 35, and 36.

CONCLUSION

Applicants have made an earnest attempt to place this case in condition for allowance. For the foregoing reasons, and for other reasons clearly apparent, Applicants respectfully request full allowance of pending Claims 2-7, 9-14, and 32-40. If the Examiner feels that a telephone conference or an interview would advance prosecution of this Application in any manner, the undersigned attorney for Applicants stands ready to conduct such a conference at the convenience of the Examiner.

Applicants believe no fees are due. However, the Commissioner is authorized to charge any fees or credit any overpayments to Deposit Account No. 02-0384 of Baker Botts L.L.P.

Respectfully submitted,

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